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OCT 26 2006

Amendment and Response

Serial No.: 09/942,200

Confirmation No.: 8194

Filed: 29 August 2001

For: DIFFUSION BARRIER LAYERS AND METHODS OF FORMING SAME

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Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the above-identified application:

Listing of Claims

1-22. (CANCELED)

23. (CURRENTLY AMENDED) A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a conformal chemical vapor deposited barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a simultaneously co-deposited platinum(x):ruthenium alloy, where x is in the range of about 0.90 to about 0.98 0.95 to about 0.995.

24. (CANCELED)

25. (PREVIOUSLY PRESENTED) The structure of claim 23, wherein x is about 0.95.

26. (ORIGINAL) The structure of claim 23, wherein the portion of the surface is a silicon containing surface.

27. (CURRENTLY AMENDED) A capacitor structure comprising:

a first electrode;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first electrode and second electrode comprises a chemical vapor deposited barrier layer of a simultaneously co-

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deposited platinum(x):ruthenium alloy, and further wherein x is in the range of about ~~0.90 to about 0.98~~ 0.95 to about 0.995

28.-29. (CANCELED)

30. (PREVIOUSLY PRESENTED) The structure of claim 27, wherein at least one of the first electrode and second electrode comprises the barrier layer of the simultaneously co-deposited platinum(x):ruthenium alloy and one or more additional conductive layers.

31. (PREVIOUSLY PRESENTED) The structure of claim 30, wherein the one or more additional conductive layers are formed from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

32. (CURRENTLY AMENDED) A memory cell structure comprising:
a substrate assembly including at least one active device; and
a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode including a chemical vapor deposited barrier layer formed of a simultaneously co-deposited platinum(x):ruthenium alloy, and further wherein x is in the range of about ~~0.90 to about 0.98~~ 0.95 to about 0.995.

33. (PREVIOUSLY PRESENTED) The structure of claim 32, wherein the capacitor includes:
a first electrode formed relative to a silicon containing region of the at least one active device;
a dielectric material on at least a portion of the first electrode; and
a second electrode on the dielectric material, wherein the first electrode comprises the barrier layer formed of the simultaneously co-deposited platinum(x):ruthenium alloy.

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34. **(PREVIOUSLY PRESENTED)** The structure of claim 33, wherein the first electrode comprising the barrier layer formed of the simultaneously co-deposited platinum(x):ruthenium alloy includes one or more additional conductive layers.

35.-36. **(CANCELED)**

37. **(CURRENTLY AMENDED)** An integrated circuit structure comprising:
a substrate assembly including at least one active device; and
an interconnect formed relative to the at least one active device, the interconnect including a conformal barrier layer formed of a simultaneously co-deposited platinum(x):ruthenium alloy, and further wherein x is in the range of about ~~0.90 to about 0.98~~ 0.95 to about 0.995.

38.-40. **(CANCELED)**

41. **(PREVIOUSLY PRESENTED)** The structure of claim 23, wherein the at least a portion of the surface defines a small high aspect ratio opening.

42. **(PREVIOUSLY PRESENTED)** The structure of claim 23, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

43. **(PREVIOUSLY PRESENTED)** The structure of claim 42, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

44. **(PREVIOUSLY PRESENTED)** The structure of claim 23, wherein the substrate assembly comprises at least one active device.

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45. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein the barrier layer comprises a chemical vapor deposited barrier layer.
46. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein the substrate assembly comprises a small high aspect ratio opening, and further wherein the interconnect is formed in the small high aspect ratio opening relative to the at least one active device.
47. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.
48. **(PREVIOUSLY PRESENTED)** The structure of claim 47, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.
49. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein x is about 0.95.
50. **(NEW)** A semiconductor device structure, the structure comprising:
a substrate assembly including a surface; and
a conformal chemical vapor deposited barrier layer over at least a portion of the surface, wherein at least a portion of the surface defines a small high aspect ratio opening, and further wherein the barrier layer is formed of a simultaneously co-deposited platinum(x):ruthenium alloy, where x is in the range of about 0.95 to about 0.995.
51. **(NEW)** The structure of claim 50, wherein the small high aspect ratio opening has a width of about 1 micron and an aspect ratio of greater than about 1.